REMARKS

The Official Action dated May 16, 2006 has been received and its contents carefully noted. In view of the following comments it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner and that the application be passed to issue.

Initially, with respect to the finality of the current Office Action, it is respectfully requested that such finality be reconsidered and withdrawn by the Examiner. Specifically, it is noted from the Advisory Action that in Section 7 thereof, the Examiner stated that for purposes of Appeal, the proposed amendments will not be entered and that the status of the claims as set forth includes claims rejected: 1-5 and 21-29 claims withdrawn from consideration: 6-20. Consequently, in order to ensure that Applicant's Request for Reconsideration was in fact entered for purposes of Appeal should this application ultimately be appealed, Applicant submitted the previously filed Request for Reconsideration with an accompanying Request for Continued Examination in order to insure full consideration of the request and to ensure that the request was properly made of record prior to any such appeal. Accordingly, it is respectfully submitted that the finality of the current Office Action is in fact improper and reconsideration and withdrawal of the same is earnestly solicited.

With reference now to page 3 of the Office Action, claims 1, 3-5, 21, 23-26, 28 and 29 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Admitted Prior Art in view of U.S. Patent No. 6,112,322 issued to McGibney et al. and U.S. Patent No. 6,037,792 issued to McClure. This rejection is respectfully traversed in that the combination proposed by the Examiner neither discloses nor suggests that which is presently set forth by Applicant's claimed invention.

As previously discussed, Applicant's claimed invention is directed to a non-volatile semiconductor memory device comprising a memory cell array having a plurality of memory cells arranged in an array, the memory cells being connected to a plurality of bit lines and word lines, a plurality of address input terminals inputting a plurality of addresses thereto, a test mode circuit for inputting a test mode signal when a signal is inputted to a predetermined terminal among the address input terminals, a row decoder connected to the test mode circuit and applying an excess voltage for a test to all the word lines in response to the test mode signal, a column decoder connected to the test mode circuit and setting all the bit lines to a non-selecting state in response to the test mode signal and a monitor terminal connected to the test mode circuit for outputting the test mode signal. Similarly, independent claim 21 is directed to a semiconductor memory device comprising a memory cell array having a plurality of memory cells, a plurality of word lines and a plurality of bit lines. A plurality of address input terminals for receiving a plurality of address signals are provided as well as test mode circuit connected to the address input terminals, the test mode circuit providing a test mode signal in response to the address signals received thereto. Also, a row decoder connected to the test circuit and the memory cell array is provided, the row decoder applying an excess voltage to all the word lines in response to the test mode signal, a column decoder connected to the test mode circuit and the memory cell array and a monitor terminal connected to the test mode circuit for outputting the test mode signal.

Additionally, as noted in Applicant's previous response, independent claim 26 recites a semiconductor memory device comprising a memory cell array having a plurality of memory cells, plurality of word lines and plurality of bit lines, a plurality of address input signals for receiving a plurality of address signals, a test mode circuit connected to the address input terminals, the test mode circuit providing a test mode signal in response to the

address signals received thereto, a row decoder connected to the test mode circuit and the memory cell array, the row decoder applying an excess voltage to all the word lines in response to the test mode signal, a column decoder connected to the test mode circuit and the memory cell, the column decoder receiving the test mode signal and a monitor bag to the test mode circuit for outputting the test mode signal. For the reasons discussed hereinbelow, it is respectfully submitted that the combination of references proposed by the Examiner, again, fails to disclose or suggest the particular features recited in each of independent claims 1, 21 and 26 as well as those claims which depend therefrom.

In the non-volatile semiconductor memory device according to the present invention, the memory device has a test mode circuit and a monitor terminal. The test mode circuit outputs a test mode signal according to a predetermined voltage being supplied to a predetermined terminal in a plurality of address input terminals. The monitor terminal is connected to the test mode circuit to receive the test mode in the nonvolatile semiconductor memory device. According to the present invention, the advantages discussed throughout Applicant's specification can be achieved.

While Applicant's admissions may disclose a nonvolatile semiconductor memory device, this disclosure clearly fails to set forth or remotely suggest that the test mode circuit outputs a test mode signal according to that a predetermined voltage being supplied to a predetermined terminal and a plurality of address input terminals. Additionally, Applicant's admissions fail to disclose or remotely suggest the monitor terminal referred to in Applicant's claimed invention. Accordingly, it is respectfully submitted that Applicant's admissions as discussed in Applicant's specification are insufficient in disclosing or rendering obvious Applicant's claimed invention.

Moreover, McClure discloses that Burn-In a Mode bar signal 58 is monitored either through a Burn In Flag 54 or a Device Pin 48. Additionally, McClure discloses that the Burn-in test mode circuit 10 is controlled by ETD pulse with a change in state of an address pin. However, it is respectfully submitted that McClure neither discloses nor remotely suggests that the test mode circuit outputs a test mode signal when a signal is inputted to a predetermined terminal among the address input terminals as recited by Applicant's claimed invention.

McGibney et al. merely discloses a control circuit CTRL receiving an initiation signal GO to control a stress test. McGibney et al. neither discloses nor suggests that the test mode circuit outputs a test mode signal according to a predetermined voltage being supplied to a predetermined terminal in a plurality of address input terminals. Consequently, McGibney et al. does nothing to overcome the aforementioned shortcomings associated with the combination proposed by the Examiner.

With reference to paragraph 5 of the Office Action, claims 2, 22 and 27 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admitted Prior Art in view of McGibney et al. and McClure as applied to claims 1, 21 and 26 above and further in view of U.S. Patent No. 5,982,677 issued to Fontana et al. This rejection is likewise respectfully traversed in that the patent to Fontana et al. does nothing to overcome the aforementioned shortcomings associated with the prior combination proposed by the Examiner.

It is noted that Fontana et al. merely discloses the structure of a regulator and clearly fails to disclose or remotely suggest that the test mode circuit outputs a test mode signal according to a predetermined voltage being supplied to a predetermined terminal in a plurality of address input terminals. Consequently, it is respectfully submitted that Fontana et

al. fails to overcome the aforementioned shortcomings associated as prior art and in Applicant's claimed invention as recited in each of independent claims 1, 21 and 26 clearly distinguishes over the combination proposed by the Examiner and are in proper condition for allowance.

Therefore, in view of the foregoing it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-5 and 21-29 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,

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